REMARKS

Claims 1-26 are pending in the present application. Claims 27-71 are cancelled herein. Claims 1-9 and 14 have been amended. No new matter has been added.

Claims 1, 2, 9, 16-18, 20, 25, and 26 have been rejected under 35 U.S.C. § 102(e) as assertedly being anticipated by U.S. Patent No. 6,643,167 B2 to Nii (hereinafter "Nii"). Claims 3-8, 10-15, 19, and 21-24 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Nii. Applicant respectfully traverses these rejections.

Applicant has amended claim 1 to recite that "the memory cell is a 6T-SRAM memory cell," which was previously recited in claim 2. It should be noted that the reference cited by the Office Action in its rejection of previous claim 2 fail to disclose such a device. The Office Action identified Figures 4, 10, 15, and 25 of Nii as identifying such a device, but these figures only illustrate a *circuit* and do not disclose all of the features of the *layout* as recited in claim 1, particularly the limitation of "wherein the memory cell has a long side and a short side, the long side being at least twice as long as the short side, a longitudinal axis of the p-well being parallel to the short side."

Claim 2 has been amended to recite another distinguishing feature of Applicant's invention, namely that the "p-well includes at least one pass gate transistor and at least one pull-down transistor sharing a common active area." This feature is not disclosed in the cited references.

Applicant has also amended claim 9 to include limitations of the base independent claim and the limitations of "wherein a short side of the p-well is shorter than a long side of the p-well, and wherein the PMOS transistors are oriented such that source-to-drain axes of the PMOS transistors are parallel to a longitudinal axis of the n-well, and wherein source/drain regions of the PMOS transistors do not overlap in a direction perpendicular to the longitudinal axis of the n-well."

The references cited by the Office Action fail to disclose such a device. In particular, the Eighth Embodiment (FIGS. 22-25), the Ninth Embodiment (FIGS. 26-28), and the Tenth Embodiment (FIGS. 29-31) assertedly illustrate a layout of an 8T-SRAM cell, but none of these

layouts illustrate all of the features recited in Applicant's amended claim 9. For example, among other things, the Eighth Embodiment fails to disclose that "the memory cell has a long side and a short side, the long side being at least twice as long as the short side;" the Ninth Embodiment fails to disclose that "the memory cell has a long side and a short side, the long side being at least twice as long as the short side, . . . wherein a short side of the p-well is shorter than a long side of the p-well;"[1] and the Tenth Embodiment fails to disclose that "source/drain regions of the PMOS transistors do not overlap in a direction perpendicular to the longitudinal axis of the n-well."

Accordingly, it is respectfully requested that the rejections of independent claims 1 and 9 be withdrawn. Claims 3-8 and 10-26 depend from and further limit independent claims 1 and 9, respectively, and accordingly, it is also respectfully requested that the rejections of dependent claims 3-8 and 10-26 be withdrawn as well.

In view of the above, Applicants respectfully submit that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicants request that the Examiner contact Applicants' attorney at the address below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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[1] The Ninth Embodiment of Nii discloses that the dimensions of the p-well are equal.